IN THE CLAIMS:

Please amend claims 1, 6, 7, and 14 as follows:

1. (Once Amended) An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines comprised of a single conductive material extending along said upper surface of said first dielectric layer, each line of said plurality of lines having upper and lower surfaces, and adjacent lines of said plurality of lines having spaces situated therebetween, the lower surfaces of each line of said plurality of lines being in contact with said upper surface of said first dielectric layer;

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the upper surface of each line of said plurality of lines; and

a dielectric material situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines.

6. (Once Amended) An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines comprised of a single conductive material extending along said upper surface of said first dielectric layer; wherein:

each line of said plurality of lines has an upper surface, a lower surface, and at least one side surface;

adjacent lines of said plurality of lines have spaces situated therebetween;

the lower surfaces of each line of said plurality of lines is in contact with said upper surface of said first dielectric layer; and

the upper surface of at least one line of said plurality of lines has thereon a layer of a refractory metal nitride;

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the upper surface of each line of said plurality of lines; and

a dielectric material situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines.

7. (Once Amended) The interlevel dielectric structure as defined in Claim 6, wherein:

said layer of refractory metal nitride has an electrical insulation layer thereon, said electrical insulation layer having thereon said second dielectric layer; and

at least one side surface of the dielectric material is in contact with at least one side surface of at least one of the plurality of lines.

14. (Once Amended) An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines comprised of a conductive material extending along said upper surface of said first dielectric layer; wherein:

each line of said plurality of lines has an upper surface, a lower surface, and at least one side surface;

adjacent lines of said plurality of lines have spaces situated therebetween;

the lower surfaces of each line of said plurality of lines is in contact with said upper surface of said first dielectric layer;

the upper surface of at least one line of said plurality of lines has thereon a layer of titanium nitride;

said layer of titanium nitride has thereon a silicon dioxide layer;

said silicon dioxide layer not being in contact with at least one side surface of

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the silicon dioxide layer of each line of said plurality of lines; and

a dielectric material, having at least one side surface, situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines, and at least one side surface of the dielectric material being in contact with at least one side surface of at least one of the plurality of lines.